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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/002,499	11/02/2001	Theodore F. Vaida	01-683	2208

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EXAMINER	
BRITT, CYNTHIA H	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 04/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/002,499	VAIDA, THEODORE F.	
	Examiner	Art Unit	
	Cynthia Britt	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 December 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

#12

DETAILED ACTION

Claims 1-21 are presented for examination.

Drawings

The drawings were received on December 13, 2004. These drawings are acceptable.

Claim Objections

The objections to claims are withdrawn based on the amendment filed December 13, 2004.

Response to Arguments

Applicant's arguments filed December 13, 2004 have been fully considered but they are not persuasive.

In response to applicant's argument that there is no suggestion (motivation) to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Sato et al. (column 2 lines 12-20) suggest that with up to 20% available space on the chip, it would make sense that those logic gates could be used to form a "block".

As per applicant's argument that the references do not teach "interchangeable hard macrocells", it seems that the language used here, such as 'interchangeable', is at issue. As applicant claims that, the macrocell can be RAM, processors, or controllers etc., it would seem that the circuitry within the macrocell is not the same type of circuit in the macrocell with which it is being interchanged. If this is not the case, the examiner suggests the use of a more descriptive term such as 'redundant macrocells', which would be used to replace a non-functional block.

Therefore, the previous rejection of claims 1-21 is maintained.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-6, 8-13, and 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sato et al. U.S. Patent No. 6,532,579 in view of Gupta U.S. Patent No. 6,681,354.

As per claims 1,8, and 15, Sato et al. substantially teach the claimed circuit and method of manufacturing and testing the circuit, in which, a semiconductor integrated circuit has a plurality of programmable logic cells where a first programmable logic unit and a second programmable logic unit which respectively comprise a plurality of programmable logic cells with storage elements and each capable of outputting an arbitrary logic output corresponding to an input are placed so as to interpose circuit blocks placed on a semiconductor chip, and the first programmable logic unit and the second programmable logic unit are capable of accessing in parallel. In a logic LSI like a system LSI configured under a CBIC (Cell Base IC) system by an arrangement of macrocells such as a CPU core, a RAM, etc., free spaces have been defined between respective circuit blocks. The total amount reaches 5 to 10% of a chip even on the average and might reach near 20% in the worst case. Converting it to the number of logic gates could yield the creation of gates approximates to four thousand to one hundred thousand in number. Therefore, since a test circuit for examining each in-chip circuit block can be configured using each of programmable logic cells provided in such free spaces, according to the above means, a self-examining test circuit can be formed, and a semiconductor integrated circuit capable of performing a non-defective product decision without using an expensive tester can be implemented. Since the test circuit is provided inside the chip, a circuit block to be tested is directly tested without being via

other circuit blocks, and even a local circuit lying inside the circuit block can directly be tested. It is also possible to effect a sufficient test on an on-chip CPU or other difficult to test circuitry. A decoder circuit capable of selecting any of the plurality of programmable logic cells, and amplifier circuits each of which writes and reads information into and from each storage element in the programmable logic cell selected by the decoder circuit, are placed at a peripheral edge portion of the semiconductor chip. Thus, an arbitrary logic circuit can be added after the use of internal programmable logic cells in each of individual chip units. The programmable logic cell constitutes a test circuit for examining at least one of the circuit blocks. Thus, a test circuit is constructed by use of internal programmable logic cells in each of individual chip units to make it possible to test the circuit blocks. The programmable logic cell may constitute a repairing circuit for mending a faulty portion, which exists in any of the circuit blocks. Figure 16 shows examples of bus connections of programmable logic. The wirings in the wiring areas VLA1, VLA2, HLA1 (figure 4) and HLA2 may be connected to signal lines constituting a system's bus so that the signals are supplied via the bus. (Column 1 line 62 through column 2 line 56, figures 4,10-12, 14, 16, and 18-19) Not explicitly disclosed by Sato et al. is that the programmable logic is in a block form.

However, in an analogous art, Gupta teaches a field programmable gate array for use in an integrated processing system capable of testing other embedded circuit components in the integrated processing system. The field programmable gate array detects a trigger signal (such as a power reset) in the integrated processing system. In response to the trigger signal, the field programmable gate array receives first test

program instructions from a first external source and executes the first test program instructions in order to test the other embedded circuit components in the integrated processing system. When testing of the other embedded circuit components is complete, the field programmable gate array loads its normal operating code and performs its normal functions. The embedded FPGA operates as follows: 1) At power-up a specific BIST device or FPGA BIST code for the FPGA checks the FPGA integrity; 2) If the FPGA passes its own self-test, a bitstream configuration (i.e., program instructions) representing the SoC BIST code for the remainder of the SoC chip is loaded into the FPGA; 3) The SoC BIST code sets up the FPGA hardware to perform an exhaustive hardware test of the system; and 4) Once the SoC BIST function is completed, the embedded FPGA can be reprogrammed to be used as a block of embedded reconfigurable FPGA logic. The field programmable gate array is capable of controlling a configurable data bus coupling the field programmable gate array to the other embedded circuit components in the integrated processing system. (Abstract, column 2 lines 10-23, and lines 50-59) Therefore, it would have been obvious to a person having ordinary skill in the art at the time this invention was made to have used the programmable logic block of Gupta with the system of Sato et al. This would have been obvious as suggested by Sato et al. (column 2 lines 12-20). With up to 20% available space on the chip, it would make sense that those logic gates could be used to form a "block".

As per claims 2, 9, and 16, Gupta teaches placing an optional FPGA BIST circuit and other peripheral circuits on the chip (column 4 lines 18-27, Figure 1). The examiner

would like to point out that it is well known in the memory art to provide additional memory blocks known as 'spare' or 'redundancy' blocks in order to repair defects in the memories of specified chips.

As per claims 3, 10 and 17, Sato et al. teach "after the examination of the circuit blocks by the test circuit configured by the programmable logic cell has been completed, a semiconductor integrated circuit judged to be defective, based on the result of examination is removed. The programmable logic cell having constituted the test circuit may have a make up of a logic circuit like a custom logic circuit having a function desired by a user. After the examination of the circuit blocks by the test circuit has been finished, a portion having a defect detected by the examination may be repaired by the programmable logic cell having constituted the test circuit or by the programmable logic cell other than the same."(Column 3 line 57 through column 4 line 5)

As per claims 4, 11, and 18, Sato et al teach "Next, circuit blocks such as macro cells such as a central processing unit CPU, a read-only memory ROM, *a static memory SRAM, a dynamic memory DRAM, a memory management unit MMU, a digital signal processor DSP,* etc. which constitute the system LSI; *a custom logic circuit (user logic) CUSTOM having a function desired by a user*; etc. are prepared (Step S2). In consideration of the forms and sizes of these circuit blocks, the placement of a bus BUS for connecting between these circuit blocks, etc., the layout of the circuit blocks on the semiconductor chip is determined as shown in FIG. 12 by way of example (Step S3)." (Column 12 line 47-57)

As per claims 4, 11, and 18, Gupta teaches, "FIG. 1 illustrates processing system 100, which includes exemplary system-on-a-chip (SoC) device 105 according to one embodiment of the present invention. SoC device 105 is a single integrated circuit comprising embedded field programmable gate array (FPGA) 115, optional FPGA built-in self test (BIST) circuit 116, peripheral circuits 120 and 125, *microprocessor* 130, random access memory (RAM) 135, read-only memory (ROM) 140, configurable bus 150, main (or system) bus 160, and bridge circuit 170. *Processing system 100 is shown in a general level of detail because it is intended to represent any one of a wide variety of electronic devices, particularly consumer appliances. For example, processing system 100 may be a printer rendering system for use in a conventional laser printer. Processing system 100 also may represent selected portions of the video and audio compression-decompression circuitry of a video playback system, such as a video-cassette recorder or a digital versatile disk (DVD) player. In another alternative embodiment, processing system 100 may comprise selected portions of a cable television set-top box or a stereo receiver.* Embedded FPGA 115 and peripheral circuits 120 and 125, which are arbitrarily labeled **Circuit Block 1 and Circuit Block 2**, respectively, *may be configured to implement any designated function in processing system 100. For example, peripheral circuit 120 may be a video codec and peripheral circuit 125 may be an audio codec. In the ordinary operation of processing system 100, embedded FPGA 115 also may be a video codec, and audio codec, or some other functional unit, such as a bus controller for configurable bus 150.*" (Column 4 lines 18-48)

As per claims 5, 12, and 19, Sato et al. teach, "Each in-chip circuit block is tested by use of the programmable logic cell." Abstract

As per claims 6, 13, and 20, Sato et al. teach that the FPGA unit is used as for the formation of the repairing circuit at the time that the defect is found out in the circuit block, yields are improved. The bus lines connect the FPGA circuitry to the logic blocks And would necessarily be used to implement testing and repair. (Column 15 line 49 through column 16 line 35, column 18 lines 50-60)

Claims 7, 14, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sato et al. U.S. Patent No. 6,532,579 in view of Gupta U.S. Patent No. 6,681,354 as applied to claims 1, 8, and 15 above, and further in view of Krick et al. U. S. Patent No. 5,638,382.

As per claims 7, 14, and 21, Sato et al. and Gupta as combined above (see rejection of claims 1,8, and 15) substantially teach the claimed circuit and methods of operating and manufacturing an integrated circuit. Not explicitly disclosed in the above combination is a memory that stores a signature for subsequent use to place the circuit into operational status.

However, in an analogous art, Krick et al. teach A processor with a built in self test function that provides intermediate self test results is disclosed including at least one logic array and a test circuit for each logic array coupled to generate a logic array signature during a built in self test of the processor. The processor further comprises a set of internal registers including a performance register that stores the logic array signature and a register that stores a pass/fail indication for the built in self test of the

processor. The internal registers also store a pass/fail indication for a cache memory built in self test and a pass/fail indication for a constant read only memory built in self test. (Abstract, figure 3, column 5 lines 6-57) Therefore, it would have been obvious to a person having ordinary skill in the art at the time this invention was made to have used the circuit/methods of Krick et al. with the systems of Sato et al. and Gupta as combined above. This would have been obvious as suggested by Sato et al. (column 1 lines 17-43) in order to implement BIST functionality without adding additional space or cost, since the circuit is being tested and repaired by the programmable logic cells, the test and repair would necessarily be implemented only once as the programmable logic cells are used in other functional means.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Cynthia Britt
Examiner
Art Unit 2133

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

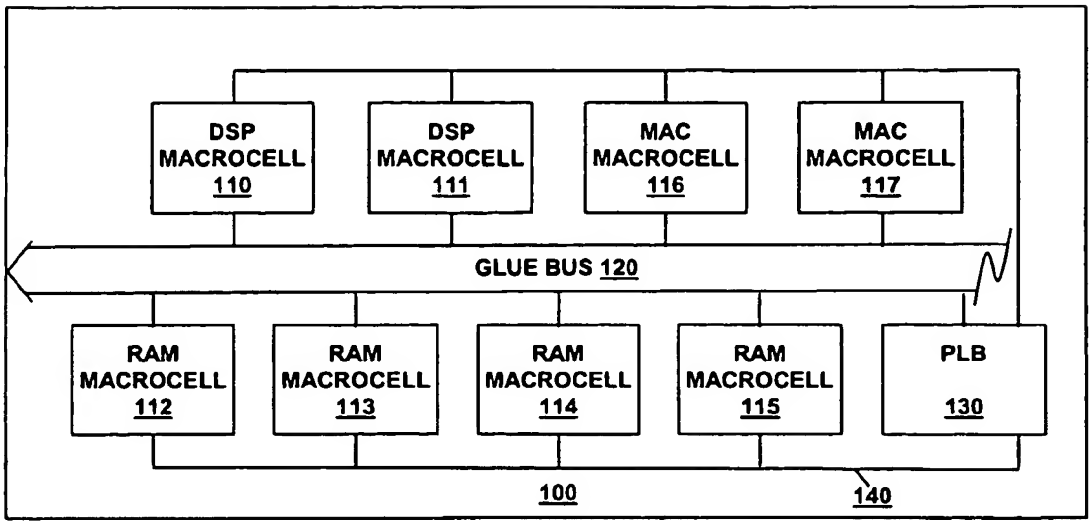

FIGURE 1

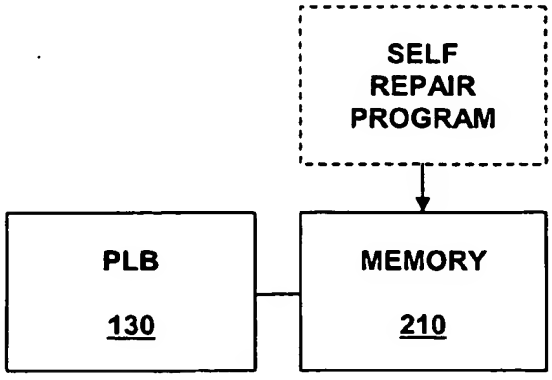

FIGURE 2

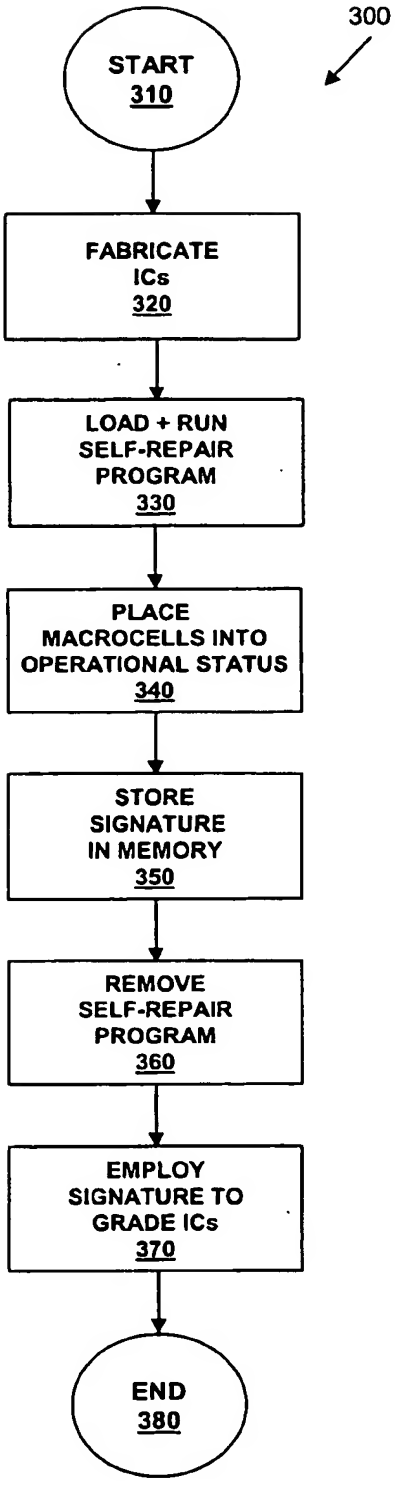

FIGURE 3

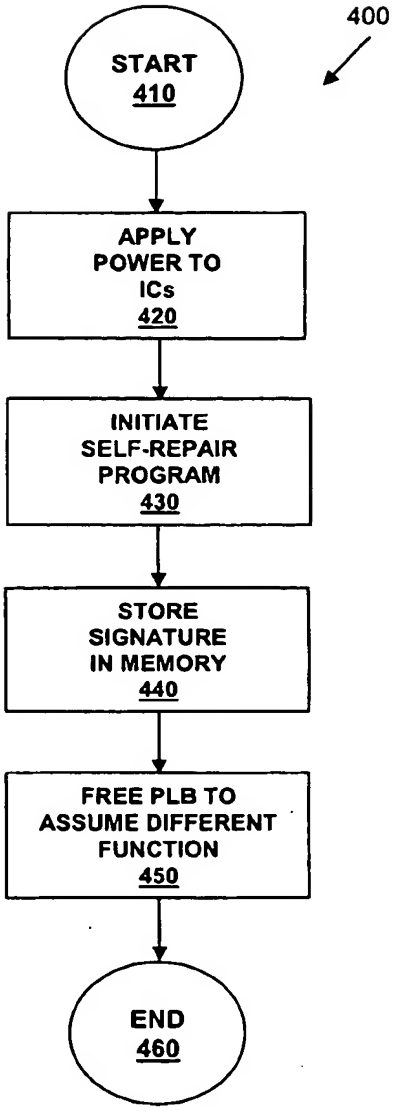

FIGURE 4